TC571000D-15, -20, -200, -25
TC571001D-15, -20, -200, -25

DESCRIPTION

The TC571000D/TC571001D is a 131,072 word × 8 bit CMOS ultraviolet light erasable and electrically programmable read only memory.

The TC571000D is JEDEC standard pin configuration and the TC571001D is compatible with 28 pin 1M bit Mask ROM. Both products are packed in 32 pin standard cerdip package.

TC571000D/TC571001D is fabricated with the CMOS technology. Advanced circuit techniques provide both high speed and low power features with a maximum operating current of 30mA/6.7MHz and access time of 150ns/200ns/250ns.

The programming times of the TC571000D/TC571001D except overhead times of EPROM programmer is only 14 seconds by using the high speed programming algorithm.

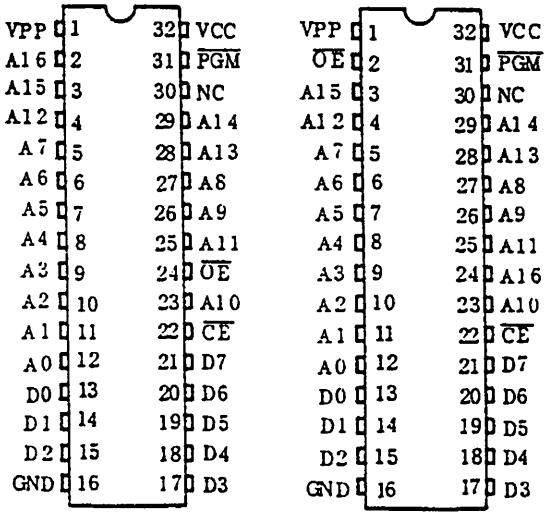
FEATURES

- Peripheral circuit: CMOS
  Memory cell : N-MOS
- Access Time

	-15	-20	-25	-200
V_{CC}	5V±5%			5V±10%
Temp	0∿70°C	-40 ∿ 85°C		0 ∿ 70°C
t_{ACC}	150ns	200ns	250ns	200ns

- Low power dissipation
  Active : 30mA/6.7MHz
  Standby: 100μA(Ta=85°C)
- Single 5V power supply
- Full static operation
- High speed programming operation: t_{PW} 0.1ms
- Input and output TTL compatible
- JEDEC standard 32 pin: TC571000D
- 1M MROM compatible : TC571001D
- Standard 32 pin DIP cerdip package

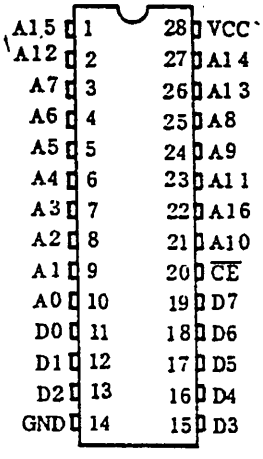
PIN CONNECTION (TOP VIEW)



TC571000D

TC571001D

(Reference)

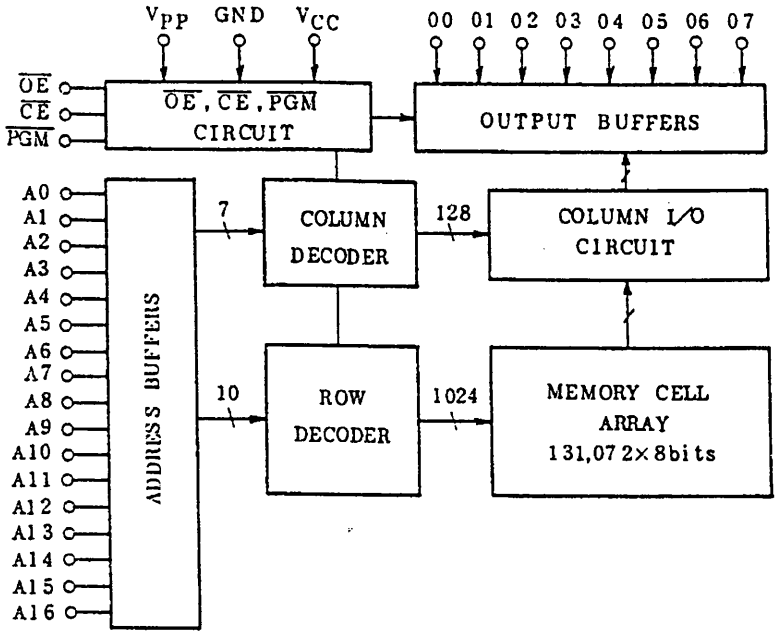


(1M Mask ROM TC531000P)

PIN NAMES

A0 ∿ A16	Address Inputs
D0 ∿ D7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{PGM}$	Program Control Input
V_{CC}	V_{CC} Supply Voltage
V_{PP}	Program Supply Voltage
GND	Ground
NC	No Connection

BLOCK DIAGRAM



MODE SELECTION

MODE \ PIN	$\overline{PGM}$	$\overline{CE}$	$\overline{OE}$	VPP	VCC	O0 ∿ O7	POWER
Read	H	L	L	5V	5V	Data Out	Active
Output Deselect	*	*	H			High Impedance	
Standby	*	H	*			High Impedance	Standby
Program	L	L	H	12.75V	6.25V	Data In	Active
Program Inhibit	*	H	*			High Impedance	
	H	L	H			High Impedance	
Program Verify	H	L	L			Data Out	

*: H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	-0.6 ∿ 7.0	V
V_{PP}	Program Supply Voltage	-0.6 ∿ 14.0	V
V_{IN}	Input Voltage	-0.6 ∿ 7.0	V
$V_{I/O}$	Input/Output Voltage	-0.6 ∿ V_{CC}+0.5	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature Time	260 · 10	°C · sec
T_{STRG}	Storage Temperature	-65 ∿ 125	°C
T_{OPR}	Operating Temperature	-40 ∿ 85	°C

READ OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TC571000D/1001D-15,-20,-25			TC571000D/1001D-200			UNIT
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
V_{IH}	Input High Voltage	2.2	-	V_{CC}+0.3	2.2	-	V_{CC}+0.3	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	-0.3	-	0.8	
V_{CC}	V_{CC} Power Supply Voltage	4.75	5.00	5.25	4.50	5.00	5.50	
V_{PP}	V_{PP} Power Supply Voltage	V_{CC}-0.6	V_{CC}	V_{CC}+0.6	V_{CC}-0.6	V_{CC}	V_{CC}+0.6	

D.C. AND OPERATING CHARACTERISTICS (Ta=-40 ∿ 85°C)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0 ∿ V_{CC}		-	-	±10	μA
I_{CCO1}	Operating Current	$\overline{CE}$=0V	f=6.7MHz	-	-	30	mA
I_{CCO2}		I_{OUT}=0mA	f=1MHz	-	-	10	
I_{CCS1}	Standby Current	$\overline{CE}$=V_{IH}		-	-	1	mA
I_{CCS2}		$\overline{CE}$=V_{CC}-0.2V		-	-	100	μA
V_{OH}	Output High Voltage	I_{OH}=-400uA		2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA		-	-	0.4	V
I_{PP1}	V_{PP} Current	V_{PP}=V_{CC}±0.6V		-	-	±10	μA
I_{LO}	Output Leakage Current	V_{OUT}=0.4V ∿ V_{CC}		-	-	10	μA

Ta=0 ∿ 70°C for TC571000D/TC571001D-15,-200

A.C. CHARACTERSITICS (Ta=-40 ∿ 85°C, V_{PP}=V_{CC}±0.6V)

SYMBOL	PARAMETER	TC571000D/1001D -15		TC571000D/1001D -20,-200		TC571000D/1001D -25		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	-	150	-	200	-	250	ns
t_{CE}	$\overline{CE}$ to Output Valid	-	150	-	200	-	250	
t_{OE}	$\overline{OE}$ to Output Valid	-	70	-	70	-	100	
t_{PGM}	$\overline{PGM}$ to Output Valid	-	70	-	70	-	100	
t_{DF1}	$\overline{CE}$ to Output in High-Z	0	60	0	60	0	90	
t_{DF2}	$\overline{OE}$ to Output in High-Z	0	60	0	60	0	90	
t_{DF3}	PGM to Output in High-Z	0	60	0	60	0	90	
t_{OH}	Output Data Hold Time	0	-	0	-	0	-	

Ta=0 ∿ 70°C for TC571000D/TC571001D-15,-200

A.C. TEST CONDITIONS

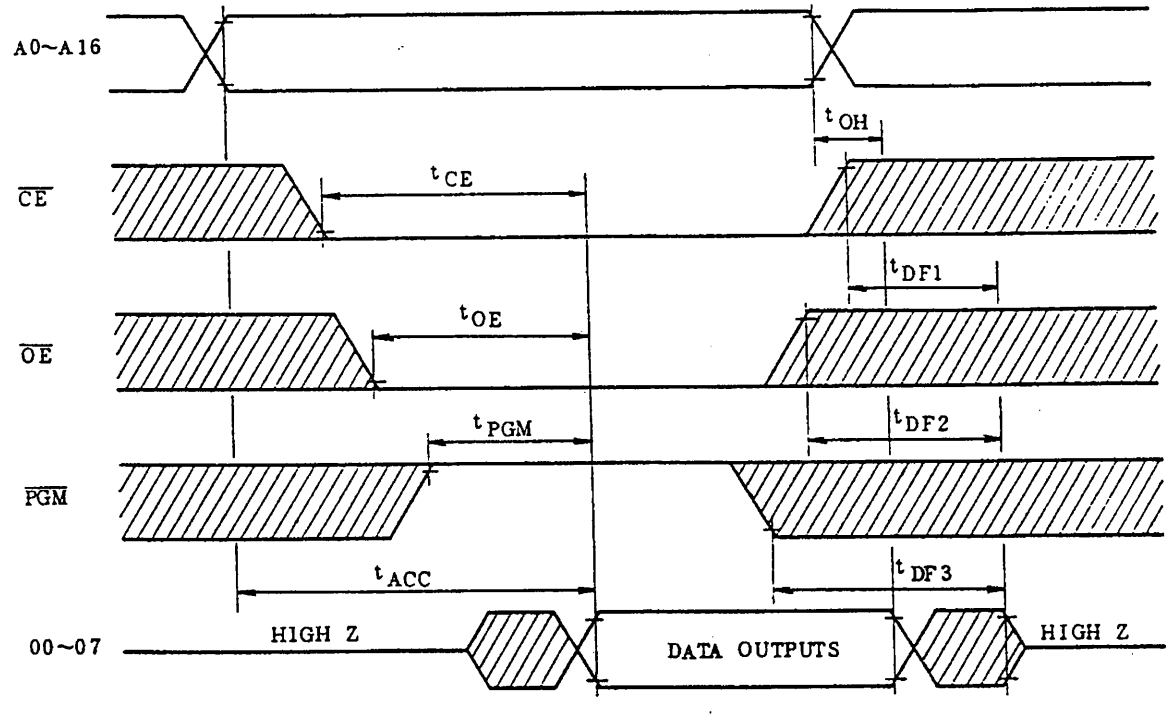
- Output Load : 1 TTL Gate and C_L=100pF
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.45V 5o 2.4V
- Timing Measurement Reference Level: Inputs 0.8V and 2.2V Outputs 0.8V and 2.0V

CAPACITANCE* (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	-	4	8	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	-	10	12	

* This parameter is periodically sampled is not 100% tested.

TIMING WAVEFORMS (READ)



HIGH SPEED PROGRAM OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	
V_{CC}	V_{CC} Power Supply Voltage	6.00	6.25	6.50	
V_{PP}	V_{PP} Power Supply Voltage	12.50	12.75	13.00	

D.C. AND OPERATING CHARACTERISTICS (T_a=25±5°C, V_{CC}=6.25±0.25V, V_{PP}=12.75±0.25V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0 ∿ V_{CC}	-	-	±10	μA
V_{OH}	Output High Voltage	I_{OH}=-400uA	2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	-	-	0.4	V
I_{CC}	V_{CC} Supply Current	-	-	-	30	mA
I_{PP2}	V_{PP} Supply Current	V_{PP}=13.0V	-	-	50	mA
V_{ID}	A9 Auto Select Voltage	-	11.5	12.0	12.5	V

A.C. PROGRAMMING CHARACTERISTICS (T_a=25±5°C, V_{CC}=6.25±0.25V, V_{PP}=12.75±0.25V)

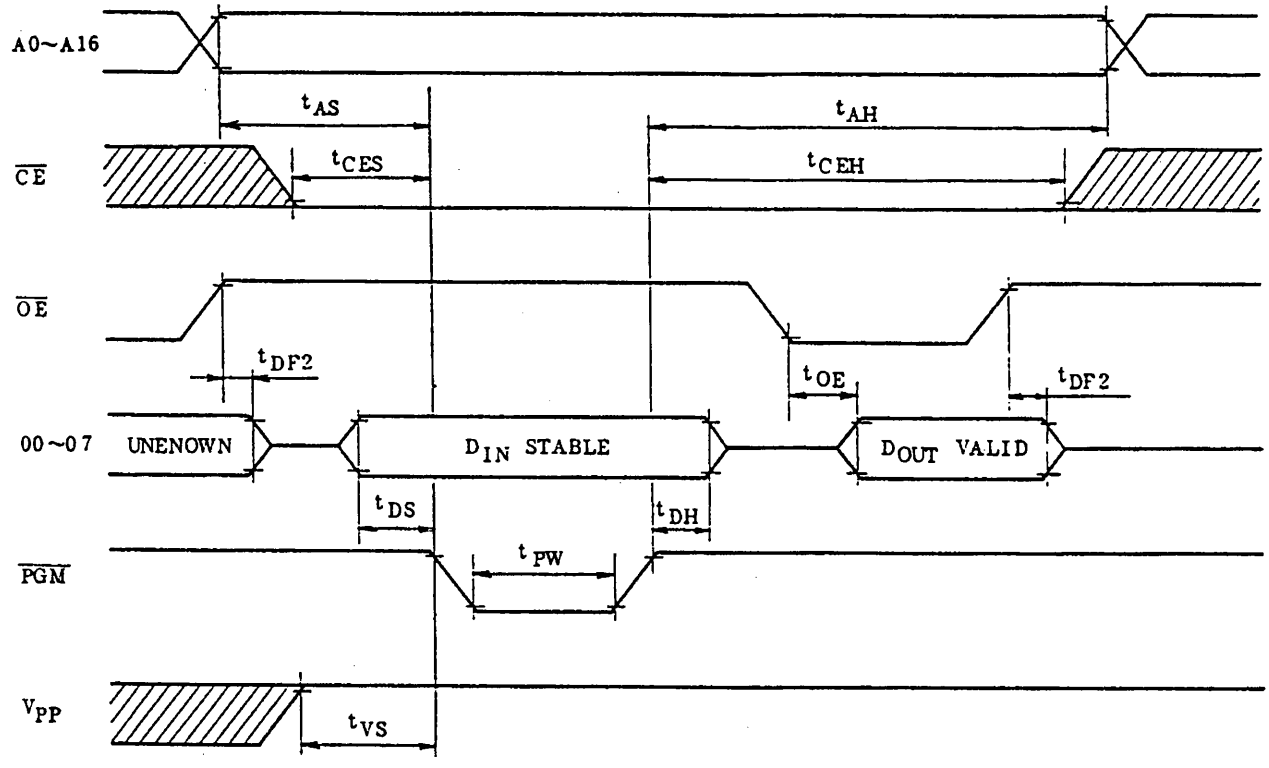
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	-	2	-	-	us
t_{AH}	Address Hold Time	-	2	-	-	us
t_{CES}	$\overline{CE}$ Setup Time	-	2	-	-	us
t_{CEH}	$\overline{CE}$ Hold Time	-	2	-	-	us
t_{DS}	Data Setup Time	-	2	-	-	us
t_{DH}	Data Hold Time	-	2	-	-	us
t_{VS}	V_{PP} Setup Time	-	2	-	-	us
t_{PW}	Program Pulse Width	-	0.095	0.1	0.105	ms
t_{OE}	$\overline{OE}$ to Output Valid	-	-	-	100	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	CE=V_{IL}	-	-	90	ns

A.C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L(100pF)
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.45V and 2.4V
- Timing Measurement Reference Level: Input 0.8V and 2.2V, Output 0.8V and 2.0V

HIGH SPEED PROGRAM OPERATION

TIMING CHART



Note: 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.

2. Removing the device from socket and setting the device in socket with V_{PP}=12.75V may cause permanent damage to the device.

3. The V_{PP} supply voltage is permitted up to 14V for program operation, so the voltage over 14V should not be applied to the V_{PP} terminal. When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

ERASURE CHARACTERISTICS

The TC571000D/TC571001D's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window. Then integrated dose (Ultraviolet light intensity [W/cm^2] × exposure time [sec.]) for erasure should be a minimum of 15 [W · sec/cm^2].
When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes. And using commercial lamps whose ultraviolet light intensity is a 12000 [μW/cm^2] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [μW/cm^2] × (10 × 60) [sec] ≅ 15 [W · sec/cm^2].)
The TC571000D/TC571001D's erasure begins to occur when exposed to light with wavelength shorter then 4000Å. The sunlight and the flourescent lamps will include 3000 ∿ 4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opeque seals - Toshiba EPROM Protect Seal AC901 - are available.

OPERATION INFORMATION

The TC571000D/TC571001D's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

		$\overline{PGM}$	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	O0 ∿ O7	POWER
READ OPERATION (Ta=-40 ∿ 85°C)	Read	H	L	L	5V	5V	Data Out	Active
	Output Deselect	*	*	H			High Impedance	
	Standby	*	H	*			High Impedance	Standby
PROGRAM OPERATION (Ta=25±5°C)	Program	L	L	H	12.75V	6.25V	Data In	Active
	Program Inhibit	*	H	*			High Impedance	
		H	L	H			High Impedance	
	Program Verify	H	L	L			Data Out	

Note: H; V_{IH}, L; V_{IL}, *; V_{IH} or V_{IL}

READ MODE

The TC571000D/TC571001D has three control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.
The output enable ($\overline{OE}$) and the program control ($\overline{PGM}$) control the output buffers. independent of device selection.
Assuming in that $\overline{CE}$=$\overline{OE}$=V_{IL} and $\overline{PGM}$=V_{IH}, the output data is valid at the output after address access time from stabilizing of all addresses.
The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).
Assuming that $\overline{CE}$=V_{IL}, $\overline{PGM}$=V_{IH} and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.
And assuming that $\overline{CE}$=$\overline{OE}$=V_{IL} and all addresses are valid, the output data is valid at the outputs after t_{PGM} from the rising edge of $\overline{PGM}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}$=V_{IH} or $\overline{OE}$=V_{IH}, the outputs will be in a high impedance state.
So two ormore ROMs can be connected together on a common bus line.
When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC571000D/TC571001D has a low power standby mode controlled by the $\overline{CE}$ signal.
By applying a high level to the $\overline{CE}$ input, the TC571000D/TC571001D is placed in the standby mode which reduce the operating current to 100μA by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC571000D/TC571001D are in the "1" state which is erased state.
Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming.
The levels required for all inputs are TTL. The TC571000D/TC571001D can be programmed any location at anytime —— either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that the desired data is correctly programmed on the programmed bits.

The verify is accomplished with $\overline{OE}$ and $\overline{CE}$ at V_{IL} and $\overline{PGM}$ at V_{IH}.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.75V) is applied to V_{PP} terminal, a high level $\overline{CE}$ or $\overline{PGM}$ input inhibits the TC571000D/TC571001D from being programmed. Programming of two or more EPROMs in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ or $\overline{PGM}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ and $\overline{PGM}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAM OPERATION

The device is set up in the high speed programming mode when the programming voltage (+12.75V) is applied to the V_{PP} terminal with V_{CC}=6.25V and $\overline{PGM}$=V_{IH}.

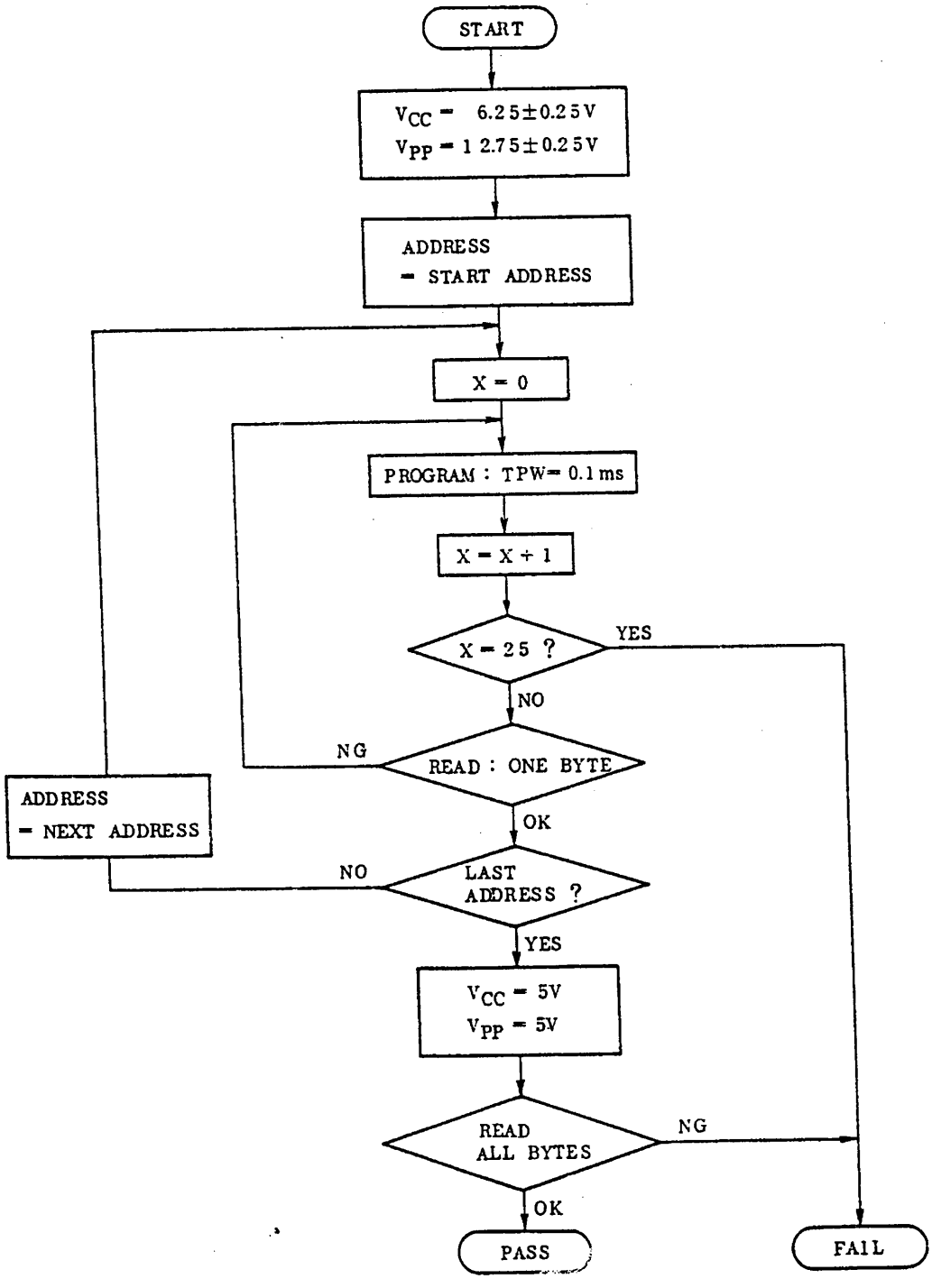
The programming is achieved by applying a single TTL low level 0.1ms pulse the $\overline{PGM}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 0.1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

When programming has been completed, the data in all addresses should be verified with V_{CC}=Vpp=5V.

HIGH SPEED PROGRAM OPERATION

FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC571000D/TC571001D which identifies it's manufacturer and device type.

The programming equipment may read out manufacturer code and device code from TC571000D/TC571001D by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH}. These two codes possess an odd parity with the parity bit of MSB (O7).

The following table shows electric signature of TC571000D/TC571001D.

SIGNATURE \ PINS		A0	O7	O6	O5	O4	O3	O2	O1	O0	HEX. DATA
Manufacture Code		V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	TC571000D	V_{IH}	1	0	0	0	0	1	1	0	86
	TC571001D		0	0	0	0	0	1	1	1	07

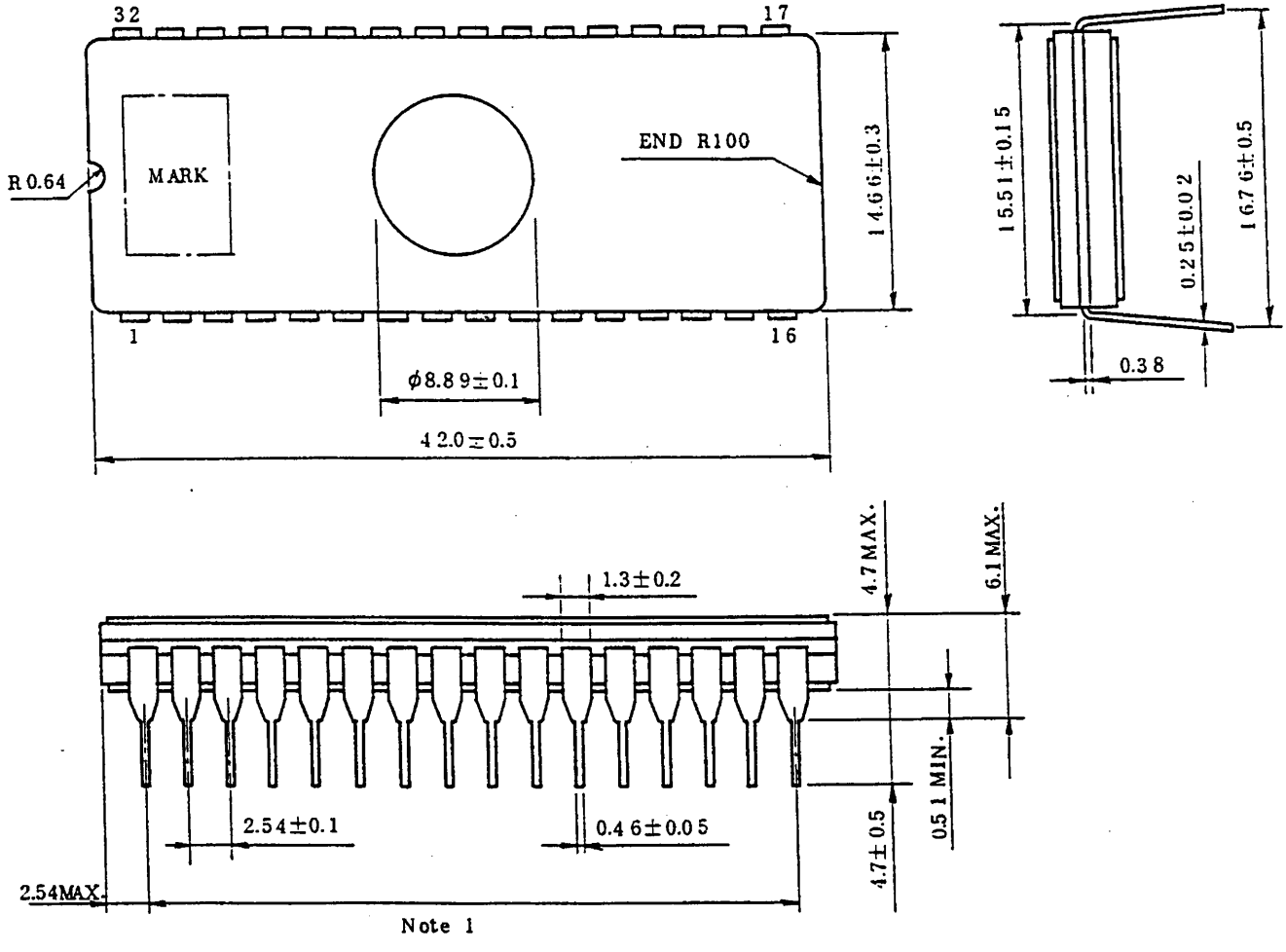
Notes: A9=12V±0.5V

A1 ∿ A8, A10 ∿ A16, $\overline{CE}$, $\overline{OE}$=V_{IL}

$\overline{PGM}$=V_{IH}

OUTLINE DRAWINGS

Unit in mm



Note 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No.1 and No.32 leads.

2. This value is measured at the end of leads.

3. All dimensions are in millimeters.

EZ0 Memory chip database
www.ezoflash.com